IN THE CLAIMS

Please add claims 34-35 and amend claims 12-13, 22, 24, and 27-28 as indicated below.

1-11. (Cancelled)

12. (Currently Amended) A processing system comprising:

a processor configured to

formulate an instruction and data, from a thread associated with a first context, for sending to a device, said instruction requesting the device to perform a command and ~~write~~ return data to ~~a destination register associated with the first context in~~ the processor;

store an indication in said first context which identifies a destination of said return data;

perform a context switch to switch from processing the first context to a second context prior to receiving the return data; and

a bus controller configured to generate a system bus operation to send the formulated instruction and data along with a thread identifier to the device.

13. (Currently Amended) The processing system of claim 12, wherein ~~the processor is further configured to store~~ said indication comprises an address of ~~the~~ a destination register.

14. (Original) The processing system of claim 13, wherein the bus controller is further configured to receive the device return data from a system bus along with the thread identifier.

15. (Previously Presented) The processing system of claim 14, wherein said processor is configured to clear a wait bit in a status register associated with the first context after writing the return data to the destination register.

16. (Original) The processing system of claim 12, wherein the device is a table lookup unit.

17. (Original) The processing system of claim 12 said processor further including:

a context register file having a separate set of general registers for the first and second contexts; and

context control registers having a separate set of control registers for the first and second contexts.

18. (Original) The processing system of claim 17, wherein the context register file includes 32 general registers for the each context.

19. (Original) The processing system of claim 17, wherein the context register file includes for each context:

a context program counter;

a context status register; and

a write address register.

20. (Original) The processing system of claim 19, wherein the context program counter holds a program counter pointing to a next instruction in an associated context.

21. (Original) The processing system of claim 19, wherein the context status register holds data that indicates whether an associated context is awaiting data from an external source.

22. (Currently Amended) The processing system of claim 19, wherein the write address register is configured to store said indication ~~stores an address of the destination register~~.

23. (Original) The processing system of claim 19 further including:
a scheduler configured to select the second context to activate.

24. (Currently Amended) The processing system of claim 23, wherein the processor is further configured to ~~further including~~:

~~means for receiving~~ receive an identifier of the second context to activate from the scheduler;

~~means for performing~~ perform a next instruction in the first context; and

~~means for pointing~~ change a processor program counter from a value associated with the first context to ~~the context program counter in the context control register~~ a value associated with the second context.

25-26. (Cancelled).

27. (Previously Presented) A method comprising:

formulating, in a processor, an instruction and data from a thread associated with a first context for sending to a device, the formulated instruction requesting the device to perform a command and ~~write~~ return data to ~~a destination register associated with the first context in~~ the processor;

storing an indication in said first context which identifies a destination of said return data;

performing, in the processor, a context switch to switch from processing the first context to a second context prior to receiving the return data; and

generating, in a bus controller, a system bus operation to send the formulated instruction and data along with a thread identifier to the device.

28. (Previously Presented) The method of claim 27 ~~further comprising storing~~ wherein said indication comprises an address of ~~the~~ a destination register.

29. (Previously Presented) The method of claim 28 further comprising:
clearing a wait bit in a status register associated with the first context after writing the return data to the destination register.

30. (Previously Presented) The method of claim 27 further comprising, in the device:
performing an operation in response to the formulated instruction and data; and
loading the return data resulting from the operation and thread identifier onto a system bus.

31. (Previously Presented) The method of claim 30 further comprising receiving the return data and thread identifier in the bus controller.

32. (Previously Presented) The method of claim 27 further comprising initiating the system bus operation in the processor before performing the context switch.

33. (Previously Presented) The method of claim 27 wherein performing the context switch comprises:
receiving an identifier of the second context;
performing a next instruction in the first context; and
changing a program counter in the processor from a value associated with the first context to a value associated with the second context.

34. (New) The processing system of claim 12, wherein in response to receiving the return data, the processor is configured to:
obtain an identity of the first context from the thread identifier;
determine said destination by accessing said first context; and
write at least a portion of the return data to the destination.

35. (New) The method of claim 27, wherein in response to receiving the return data, the method further comprises:

obtaining an identity of the first context from the thread identifier;

determining said destination by accessing said first context; and

writing at least a portion of the return data to the destination.